Design and Mathematical Analysis of a Single-Phase PV Residential Micro-Inverter

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ABSTRACT:

Photovoltaic (PV) system architectures are being designed to optimize energy extraction. Micro-Inverter (µI) architectures are gaining in popularity as they are increasing the efficiency and the power extracted from the PV module and mitigating the shading effect. This work details the design of a proposed DC-AC µI. The design incorporated a combination of a virtual DC bus inverter and a proposed three-winding coupled transformer which is based on a Y-source impedance configuration. High voltage spikes and low voltage regulation arises from loosely coupled inductors in the ferrite core. On the other side, transformer elimination in the µI configurations can generate high common-mode voltage as a consequence, leakage current can cause distortion of the grid current. In this paper, the developed transformer with less µI can overcome all the drawbacks mentioned above. The proposed µI has been created and designed to remove both leakage inductance and leakage current caused by a transformer-less µI configuration. In addition, the converter greatly reduced component stress and increased the converter voltage gain

capability in a single stage. Using Mathematica 11.2 software, a thorough mathematical model of the μI was built and proved. To assess the performance and demonstrate the features, PLECS 4.2 simulation software has been used, which shows a preference for the proposed μI over the traditional impedance source inverters in terms of boosting capability and components voltage stress.

الخلاصة:

يتم تصميم بنيات أنظمة الخلايا الكهروضوئية لتحسين استخراج الطاقة. تكتسب معماريات العاكس الصغير (μI) شعبية لأنها تزيد من الكفاءة والطاقة المستخرجة من الوحدة الكهروضوئية وتقلل من تأثير التظليل. يوضح هذا العمل تفاصيل تصميم μI DC-AC المقترح. تضمن التصميم مزيجًا من عاكس ناقل افتراضي للتيار المستمر ومحول مقترن بثلاث لفات يعتمد على تكوين مقاومة مصدر Y. تنشأ طفرات الجهد العالي وتنظيم الجهد المنخفض من المحرِّضات المترابطة بشكل فضفاض في Ferrite Core. على الجانب الآخر ، يمكن أن يؤدي التخلص من المحولات في تكوينات μI إلى توليد جهد عالٍ في الوضع المشترك نتيجة لذلك ، يمكن أن يتسبب تيار التسرب في تشويه تيار الشبكة. في هذا البحث ، يمكن للمحول المطور بأقل من μI التغلب على جميع العيوب المذكورة أعلاه. تم إنشاء وتصميم μI المقترح لإزالة كل من محاثة التسرب وتيار التسرب الناجم عن تكوين μI غير المحول. بالإضافة إلى ذلك ، قلل المحول بشكل كبير من إجهاد المكونات وزاد من قدرة المحول على اكتساب الجهد في مرحلة واحدة. باستخدام برنامج Mathematica 11.2 ، تم بناء نموذج رياضي شامل لـ μI وإثباته. لتقييم الأداء وإثبات الميزات ، تم استخدام برنامج محاكاة PLECS 4.2 ، والذي يوضح تفضيل μI المقترح على محولات مصدر الممانعة التقليدية من حيث تعزيز القدرة وضغط الجهد للمكونات.

KEYWORDS: Micro-Inverter, Photovoltaic, Inverter, Three-winding coupled transformer, Voltage stress, PWM.

1. Introduction

The rapid decline in fossil fuel supplies has developed an urgent need to use alternative and renewable energy sources to satisfy the future of rapid consumption and population growth. The solar energy has become the most popular among the different energy sources available since it is clean, abundant, and free. In general, there are three ways to use solar energy to grow biomass, to gather heat from the sun in solar thermal systems, or to convert solar irradiation into electricity in photovoltaic PV systems. Solar PV technology has gotten a lot of attention among renewable energy options because of benefits like high availability, low maintenance costs, quiet operation, and scalability. The use of the PV system as an energy source is a critical approach to the growth in the energy demand [1]. Solar panels are used in PV systems to provide usable electric power, and these solar panels are normally equipped with an inverter to convert their output DC power into AC power, which is then fed back to users via an electric power grid [٢].

The inverters are used in the PV systems to convert the Direct Current (DC) from the PV modules to Alternating Current (AC), which can feed into the grid [5]. Four different configurations are available for grid-connected PV systems as

shown in Fig.1. Central Inverter, String Inverter, Inverter with Power Optimizers, and µI [3] and [4]. The PV converter systems now on the market can be divided into three categories: (i) large-scale power generation using grid-connected systems with output powers ranging from tens of kilowatts to megawatts, (ii) Residential and commercial applications employing grid-connected systems with output power capacities less than 10 kilowatts, and (iii) remote region applications using stand-alone systems with a smaller PV plant to supply local loads. Currently, just 10.2 per cent of PV installations are stand-alone systems, with the bulk (89.8%) being grid-connected systems [5].

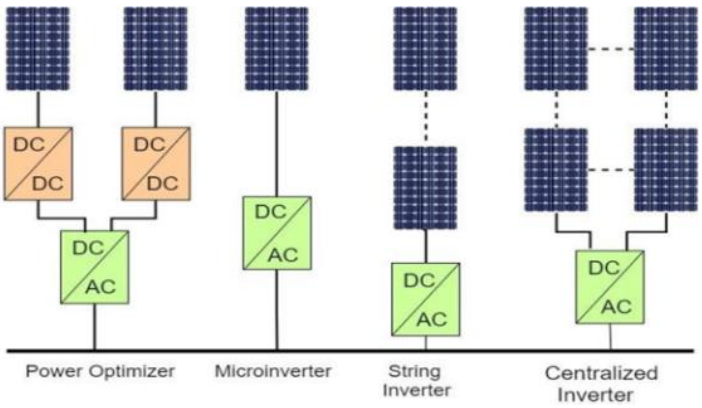

Fig.1. Different grid-tied PV inverter topologies.

The focus of this paper is on residential single-phase applications that based on the direct connection of the PV panel to

the grid through single-stage converter which is called µI. µIs are usually for individual panels with an output power level of less than 500W. The output is commonly single phase AC, which can be connected to the grid [5].

2. Literature Review

H. Liu et al., 2018 [6]: A high step-up YSI has been proposed in this study. In this topology high number of turn ratios is required to provide a voltage gain. However this leads to increase leakage inductance, which result to decrease the efficiency of the converter. This research proposed a novel arrangement that ensures a significant voltage gain by reusing the leakage energy.

L. Hongpeng, R. Yan, L. Kuan, W. Wei, and X. Dianguo, 2018 [7]: In this work an improved single-phase Y-source transformer-less PV grid connected have been proposed. In this work the YSN used for boosting the voltage of the PV modules. While the virtual DC bus inverter configuration is used at the output to eliminate the leakage current. The leakage current were eliminated by connected the PV array's negative pole is connected to the grid utility’s neutral pole.

From previous literature, this work proposed a single-stage transformer-less inverter that can be used as µI so that

avoid all the drawback of the previous work such as eliminate the leakage current and leakage inductance effect with lower voltage spike and higher voltage gain. The next section contains more information on the paper's significant contributions.

3. CONFIGURATION OF THE PROPOSED TOPOLOGY

Fig.2 depicts the proposed μI. It has an impedance source, a virtual DC bus inverter, a resistive load, and an LC output filter. Three capacitors, two passive diodes, an input inductor (Lin), and three winding coupled inductors wound in a single magnetic core make up the impedance-Source network. Five switches and a capacitor C4 make up the virtual DC bus inverter (floating capacitor). As shown in Fig.3, the positive lead of the floating capacitor was connected to the common point between S2 and S4, while the negative lead was connected to the common point between S3 and S5.

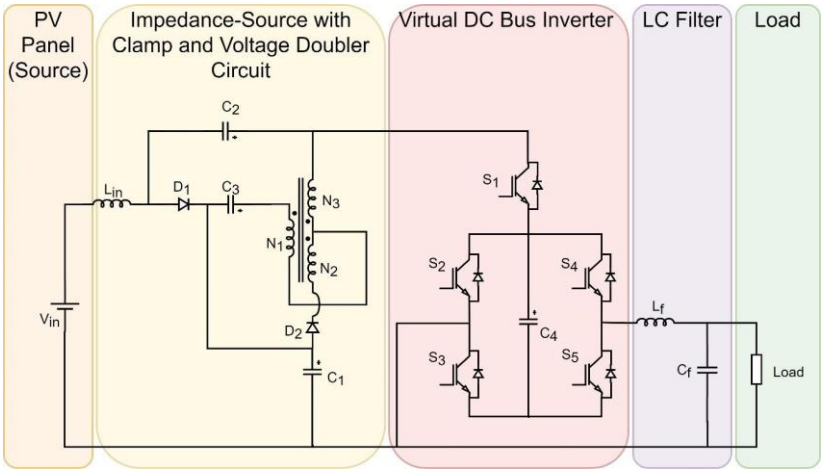

Fig.2. Proposed Single-Phase PV Residential µI.

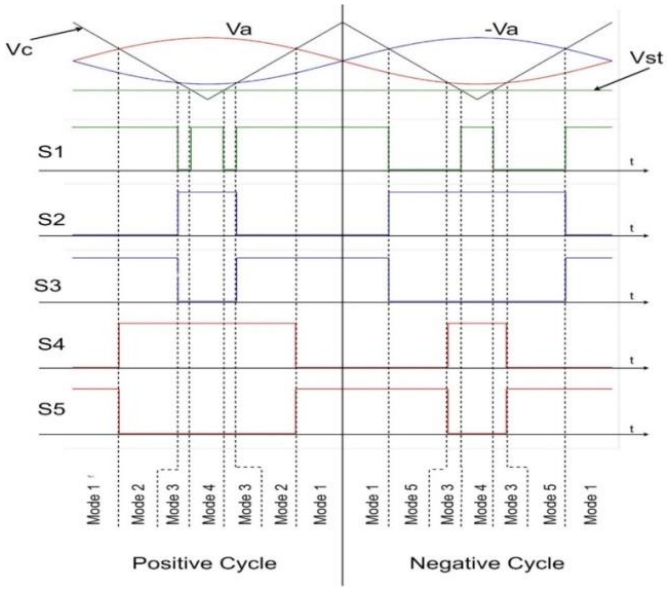

Fig.3. Modulation strategy of the proposed single-phase PV residential µI.

4. THE OPERATION MODES

The redesigned unipolar sinusoidal Pulse Width Modulation (PWM) switching pattern is depicted in Fig.3. For

modulating switches S2 and S3, the reference signal Va is compared to the carrier signal Vc, whereas -Va is used to modulate switches S4 and S5. For shoot-through time intervals, Vst stands for "reference signal". Because the floating capacitor provides the virtual DC-link voltage in the PWM approach, the switches in the same leg cannot be turned on simultaneously. S3 commutates complementary to S2 in the updated PWM, whereas S5 commutates complementary to S4 in the original PWM. S1 and S3 both commutate at the same time. Furthermore, when the Vst is greater than the Vc in the freewheeling mode with S2 and S4 conducting, S1 begins to conduct again. The machine's operating modes:

Mode 1: This is the freewheeling Mode, where S1, S3, and S5 are turned on and S2, S4 are turned off. The diode D2 is reversed-biased because the voltage total of the capacitor C3, inductor N2, and N3 is larger than the voltage of capacitor C1. The input source and input inductors Lin charge the capacitor C1, while inductors N1 and N3 charge the capacitors C2 and C3. Meanwhile, the input source, inductors Lin, N1, and N3, charge the capacitor C4.

Mode 2: This Mode is only active during the positive half of the cycle. Switches S1, S3, and S4 are ON in this Mode, while S2

and S5 are OFF. The input source and inductors charge the capacitors C1, C2, C3, and C4 similarly to Mode 1.

Mode 3: also known as freewheeling Mode, this Mode turns ON S2 and S4 while turning OFF S1, S3, and S5. The capacitor C1 discharges the input source and input inductors Lin. In the meantime, the inductors N1 and N3 charge the capacitors C2 and C3.

Mode 4: S1, S2, and S4 are turned ON, while S3 and S5 are turned OFF, in what is known as shoot-through (ST) Mode. Because the voltage of capacitor C1 is larger than the input source voltage when combined with the voltage of the inductor Lin, the diode D1 is blocked. Through switches S1 and S2, the inductor N3 discharges the capacitor C1, while the input source and capacitor C2 charge the inductor Lin. In addition, the inductors N1 and N2 drain the capacitor C3.

Mode 5: This Mode, also known as active mode, persists exclusively during the negative half of the cycle. S2 and S5 are turned ON, but S1, S3, and S4 are turned OFF. The input source and the inductors charge the capacitors C1, C2, and C3. Meanwhile, the capacitor C4 provided the load with the necessary voltage.

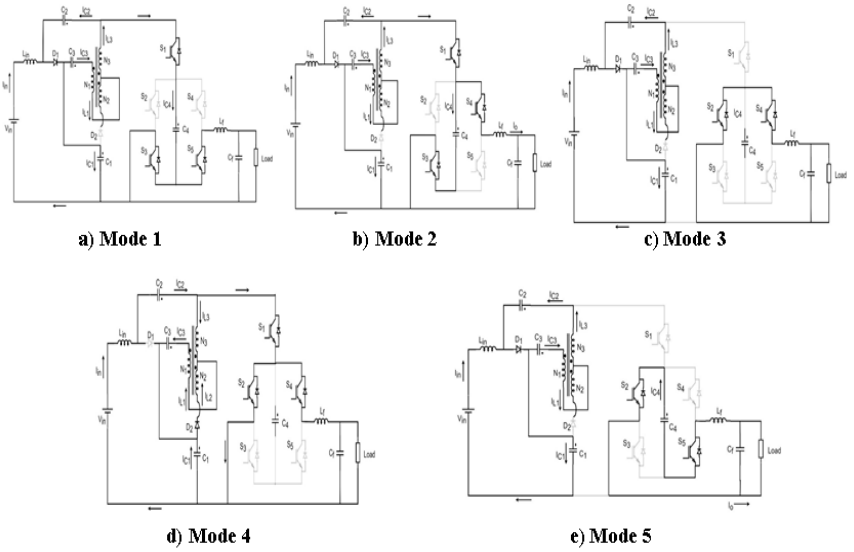

Fig.4. The equivalent circuits of the proposed μI during five mode. (a) Mode 1, (b) Mode 2, (c) Mode3 (d) Mode 4, (e) Mode 5.

I. Voltage analysis

1. Shoot-Through Mode (ST)

Fig.5a shows the equivalent circuit in ST mode. Turning ON the switches S1 and S2 at the same time will put you in ST mode. While diode D2 is conducting, diode D1 is reverse biased. In this form, the circuit equations can be represented as follows: (1)-(3):

$$V_{C3} - \frac{N_1}{N_3} V_{Lm} - \frac{N_2}{N_3} V_{Lm} = 0 \qquad (1)$$

$$V_{in} - V_{Lin} + V_{C2} = 0 \qquad (2)$$

$$V_{C1} + \frac{N_2}{N_3} V_{Lm} - V_{Lm} = 0 \qquad (3)$$

2. Non-Shoot-Through Mode

Fig.5b depicts the analogous circuit in this manner. The diode D1 is forward based in NST mode, while the diode D2 is blocking. Capacitors C1, C2, C3, and C4 are charged in this mode, while inductors are discharged. The following equations (5)-(6) can be derived when in NST mode:

$$V_{C2} + V_{Lm} + \frac{N_1}{N_3} V_{Lm} - V_{C3} = 0 \qquad (4)$$

$$V_{in} - V_{Lin} - V_{C1} = 0 \qquad (5)$$

$$V_{DC} - V_{C1} - V_{C3} + \frac{N_1}{N_3} V_{Lm} + V_{Lm} = 0 \qquad (6)$$

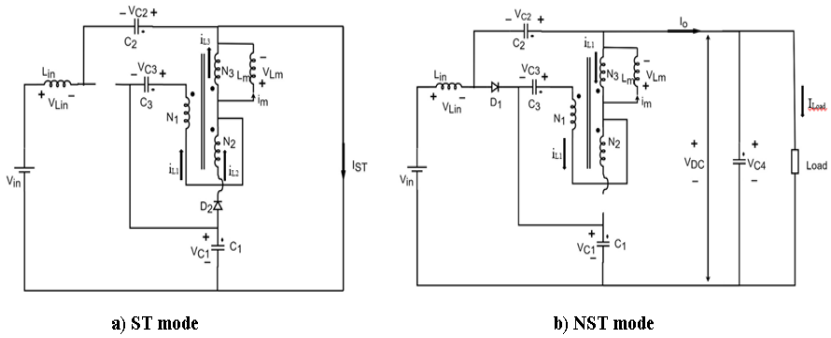

Fig. 5. Equivalent circuit of the proposed µI.

Using the circuit formulas in ST mode or DT time interval and non-shoot-through mode or (1-D) T time interval, the capacitor voltage and boosting factor of the proposed inverter can be driven.

By applying the voltage second-balance to equ. (1) and (4). The voltage of capacitor C3 can be calculated as follows:

$$V_{C3} = \frac{(1-D)(K-1)V_{in}}{1-(1+K)D} \qquad (7)$$

Where: $K = \frac{N_3+N_1}{N_3-N_2}$

Similarly, for equations (2) and (3), the voltage second-balance can be used (5). The voltage of capacitor C2 can then be determined:

$$V_{C2} = \frac{(D+K-1)V_{in}}{1-(1+K)D} \qquad (8)$$

Equations (1) and (3), as given below, can be used to calculate the voltage across C1.

$$V_{C1} = \frac{(1-D)V_{in}}{1-(1+K)D} \qquad (9)$$

This equations (7, 8, and 9) represent capacitors voltage (V_{C1},V_{C2}, and V_{C3}).

$$V_{DC} = V_{C4} = \frac{KV_{in}}{1-(1+K)D} \qquad (10)$$

The equation (10) represent output voltage in term of input voltage, Shoot-through duty ratio and winding factor.

Thus, Eq. (10) may be used to get the boosting factor, which is equal to the DC-link voltage divided by the input voltage.

$$B = \frac{V_{DC}}{V_{in}} = \frac{K}{1-(1+K)D} \qquad (11)$$

ooo

The inverter's winding factor K is determined throughout the design process. As a result, the suggested inverter's boosting factor was solely dictated by the value of the ST duty cycle. The output voltage can be increased by increasing the duty cycle D. Fig.6 depicts the proposed µI boosting factor for various duty cycles and winding factors.

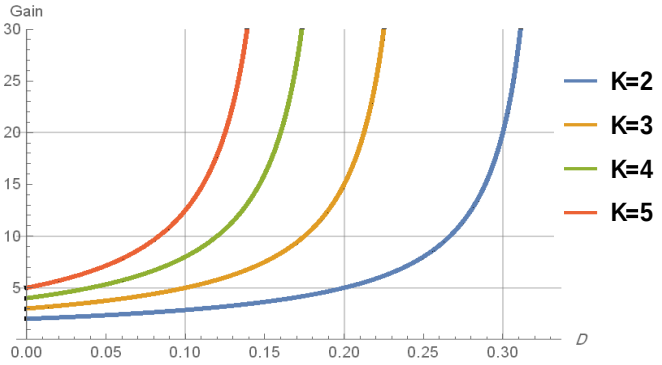

Fig. 6. The Boost factor capability of the proposed topology at different D and K.

The suggested inverter's AC output voltage can be calculated as follows:

$$V_{AC} = BMV_{in} = \frac{K}{1-(1+K)D} MV_{in} \qquad (12)$$

The modulation index is denoted by the letter M. The maximum modulation index for the ST can be calculated as follows:

$$M = 1 - D \qquad (13)$$

II. Current analysis

By simplifying the equation using Mathematica 11.2

software and do some substitution, the relationship between average magnetizing current and average input current can be obtained as:

$$I_m = \frac{I_{in}(N_1 + N_3)}{N_3} \quad (14)$$

$$I_o = \frac{(1 - 2D)I_{in}}{1 - D} \quad (15)$$

5. SIMULATION AND EXPERIMENTAL RESULTS

The proposed topology is simulated and tested to confirm the theoretical analysis below, and the circuit parameters are listed in Table 1.

Table 1. Parameters that used for simulation analysis.

Parameter		The Proposed μI
Input voltage (Vin)		25V
Output voltage (V)		30 V r.m.s
Inductors	**Lin**	3mH
	Lf	3.3mH
	N1	15
	N2	15
	N3	45
Capacitors	**C1**	220uF
	C2	220uF
	C3	220uF
	C4	940uF
	Cf	10uF
K		2
Power		25W
Operation frequency		50 Hz
Switching frequency		10 kHz

I. Simulation Results of the Proposed MI

In order to evaluate the improvement achievable with the proposed µI. The proposed topology with USPWM signals has been implemented using PLECS simulation software. Two topologies have compared with the same inverter configuration (Virtual DC Bus Inverter) at the output. Fig.7 shows the whole simulation scheme.

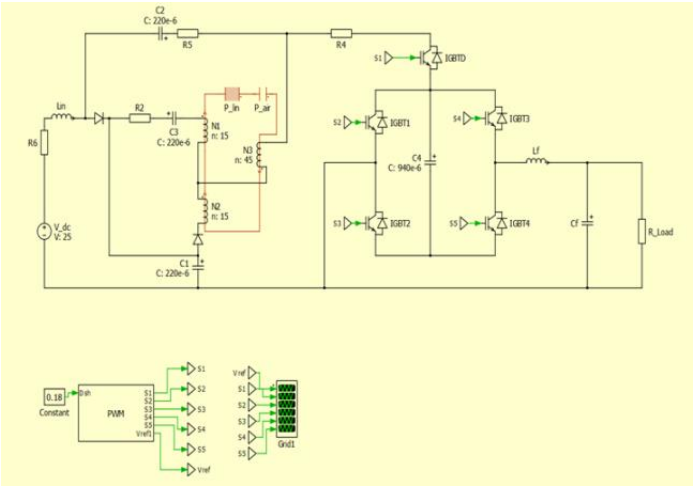

Fig.7. PLECS model of the proposed µI Power circuit.

In this section simulation results of the proposed µI are presented and compared with the YSI to illustrate the features and differences. Fig.8 shows the DC-link voltage of the proposed µI.

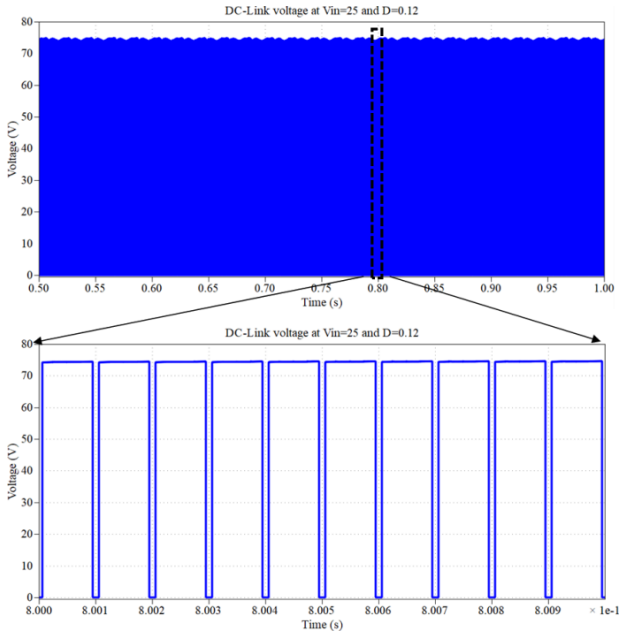

Fig.8. The proposed µI operating in two modes, shoot-through mode and active mode, produced simulation results (non-shoot-through mode). Vin=25V, K=2 and D=0.12 DC-link voltage.

The simulation results confirmed the theoretical analysis that have been driven in section 4. According to the mathematical study using eq. (10) for Vin=25V, K=2 and D=0.12, the DC-link voltage is 78V. However, as shown in Fig.8, the DC-link voltage simulation result was around 75V. The reduction voltage that shown in the PLECS simulation is due to the voltage drops across the converter components thus PLECS provided more realistic results with fast simulation time.

The simulation result of the classic YSN DC-link voltage with the virtual DC bus inverter is shown in Fig.9. The simulation was run with the same parameters as the suggested µI: Vin=25V, K=2, and D=0.12. It can easily be seen that the DC-link voltage of YSI is nearly half of that of the suggested µI, which is measured at 38V.

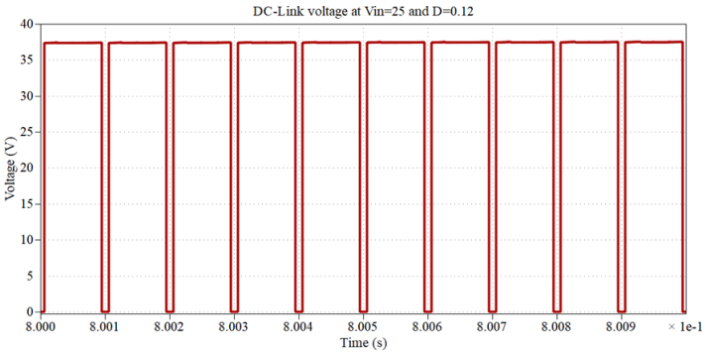

Fig.9. Results of simulations using the YSI in two modes: shoot-through mode and active mode (non-shoot-through mode). Vin=25V, K=2 and D=0.12 DC-link voltage.

The output voltage of the µI fed into LC filter in compared to the filtered output voltage of YSI is shown in Fig.10. It's clear that the peak output voltage (44V) of µI is greater than the peak output voltage of YSI (22V) for the same D. Fig.11 depicted the output current comparison of the proposed µI with YSI.

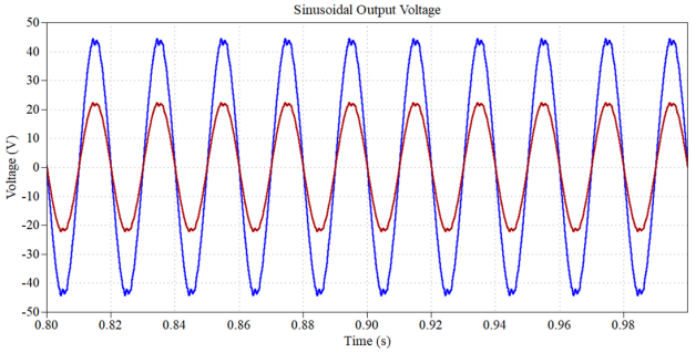

Fig. 10. Simulation comparison of the output voltage between the proposed µI and YSI at Vin = 25V, K = 2 and D = 0.12.

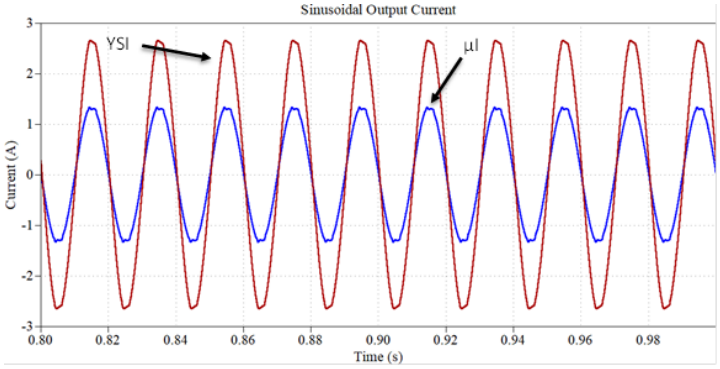

Fig. 11. The Simulation comparison of the output current between the proposed µI and YSI at Vin = 25V, K = 2 and D = 0.12.

In contrast to the traditional YSI, As shown in Fig.12, the suggested µI exhibit reduced voltage stress across the diode D1, indicating that the voltage stresses across the YSI diode D1 are nearly 5 times more than the proposed µI at the same output voltage, which is one of the most critical aspects that this topology solves. In other words, the voltage stresses across the diode D_1 is equal to the DC-link voltage for the proposed µI

while in YSI the voltages stresses across the diode D_1 is five times of the DC-link voltage.

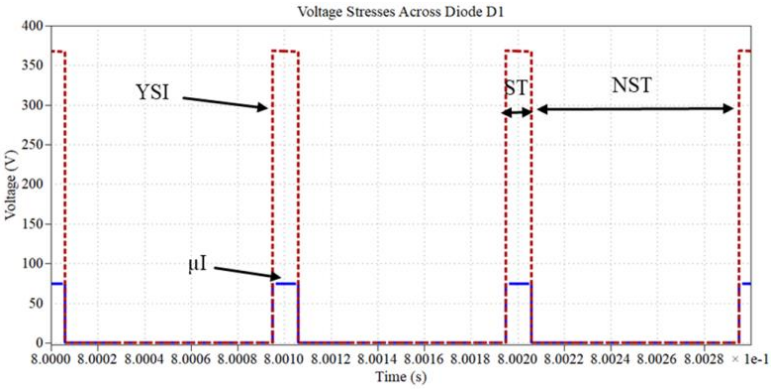

Fig.12. The Simulation results of voltage stress across diode D_1. Both topologies compared at the same RMS output voltage (30 V).

The input current comparison is shown in Fig.13. Both of the topologies have same input current equal to about 0.5A. Both of the topologies have ripple current less than 0.5A at V_{in} =25V and D=0.12. As a result, the suggested converter inherits all of the benefits of the classic YSI converter, which can realize the operation in the continuous current mode with low current ripple.

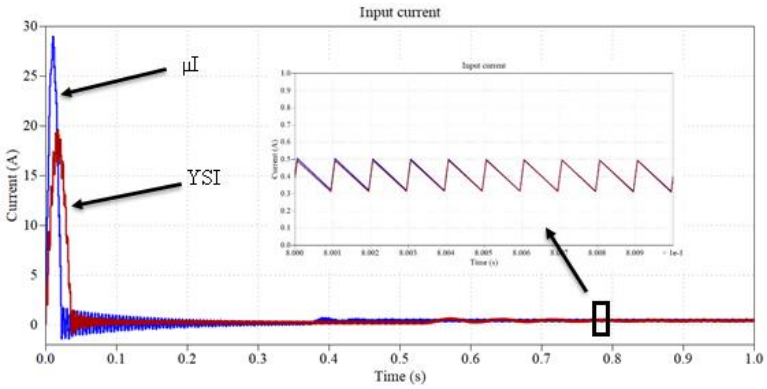

Fig.13. Simulation results of input currents. The proposed µI at K=2 compared to YSI at K=5 and both at D=0.12 and Vin=25V.

6. CONCLUSION

Based on impedance source configuration, this paper provides a revolutionary transformer-less single-stage µI architecture. At the same number of turns ratio, the suggested µI delivers twice as much voltage gain as a typical Y-source inverter. The coupling inductors leakage inductance is reduced as a result of this. Furthermore, the PV panel's negative pole is directly connected to the neutral line, fully avoiding leakage current. Because active clamping is employed to decrease leakage current, there is no requirement for a passive snubber circuit.

Even with a modest load and a ripple current of less than 0.5A, the suggested converter operates in continuous conduction mode. The despite this, due to the use of one more

capacitor, the impedance source arrangement offers blocking DC coupling for the ferrite core. Because of these features, the suggested µI is better suited to PV residential applications. Finally, simulation results confirmed the proposed µI mathematical model.

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